Zimbabwe Journal of Science & Technology pp 132-141 Vol.11 [2016]
e-ISSN 2409-0360
Zimbabwej.sci.technol

Field Programmable Gate Array Based Variable Speed Drive for a Three-Phase Induction Machine.

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ABSTRACT

In this article, the design of a Field Programmable Gate Array (FPGA) based Variable Speed Drive (VSD) is presented. The design is expected to lower VSD design costs through design integration, reduced time to market and meeting high performance drive requirements. An embedded soft processor, Altera Nios II, responsible for handling motor control algorithm written in C programming language and developed on eclipse integrated development environment is implemented in the controller. Other components like the Insulated Gate Bipolar Transistor (IGBT) control module are written in Very High Integrated circuit Hardware Description Language, generally abbreviated as VHDL, and implemented together with the Altera Nios II processor in Quartus II Computer Aided Design (CAD) software to make a System on Chip (SoC). The output IGBT control module drives the switching devices via opto-couplers. The power circuit is divided into three blocks namely; the rectifier, filter and inverter. Rectification of the AC input voltage of constant amplitude and frequency coming from the power grid is the first stage. This is done by a single phase bridge rectifier. Inversion of the voltage coming from the DC bus into an alternating signal of variable amplitude and frequency by a three phase inverter is the last stage. The FPGA based drive is designed, implemented and tested on a three phase squirrel cage induction machine. Speed control of the motor is achieved by varying the frequency of the supply using FPGA based inverter control.

Keywords: FPGA, VSD, VHDL, motor control algorithm, computer aided design, System on Chip.

Received: 24.02.2016. Accepted:20.12.2016.

1. INTRODUCTION

The architecture of today's variable speed drives is typically multi-chip. They consist of high speed Digital Signal Processors (DSPs) for fast math-intensive computation, an Application-Specific Integrated Circuit (ASIC) for industrial networking, and a processor to run the slower control loops and do all the other interfacing and Input/Output (I/O) functions. Microcontroller Units (MCUs) and DSPs, being sequential machines, have difficulty in time keeping when very high-speed runtime updates are needed in certain motor control algorithms. The trend for next generation drives calls for a more integrated solution that brings together the performance of an embedded dual-processor system, DSP blocks capable of floating point computation, and the scalability to add multiple motors in the same drive, thus lowering the cost per motor. Field Programmable Gate Arrays (FPGAs) are the ideal solution for these next generation drives as programmability provides the ability to integrate more functions for additional flexibility and scalability. FPGAs also execute multiple operations in parallel unlike MCU and DSP. The parallel nature of FPGA operation allows for higher speed computations therefore improving the control performance. This work is a presentation of the design and implementation of an FPGA based variable speed drive. Figure 1 shows the block diagram of the Variable Speed Drive (VSD) design.

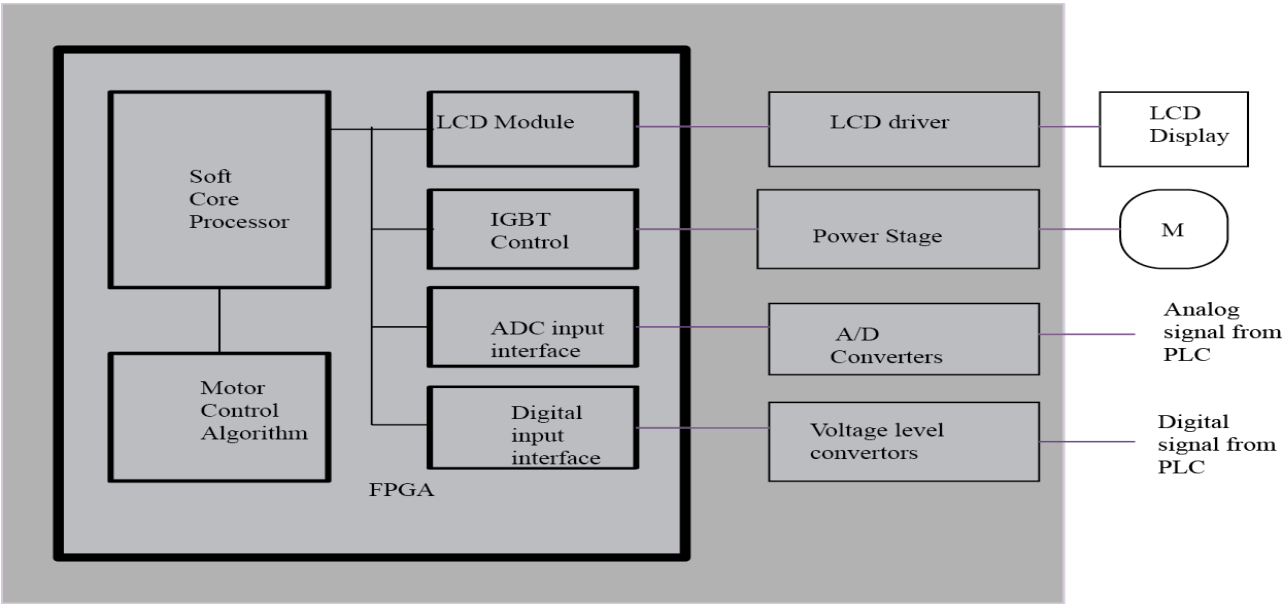

Figure1. Block Diagram of the Designed VSD

1.1 Overview

This section serves to highlight the current technologies in embedded industrial systems mainly focusing on variable speed drives. Attention has been given to industrial motors, construction of the variable speed drives, FPGAs and System on Chip (SoC) development. The outcome of much research into why FPGAs should be implemented on industrial embedded systems together with basic principles of VSDs, also known as Variable Frequency Drives (VFDs), is included.

1.1.1 Industrial Motor Control

Motors account for more than 66% of the electrical power consumed in industrial markets (Altera Corporation, 2015), (IEA, 2014, ABB Review 2015). As the cost of power continues to rise and the automation of factories increases, motor efficiency is becoming increasingly important. To achieve optimum efficiency motor control electronics has to read current and voltage of the motor and perform a series of mathematical operations using computed errors and corrections. The output results in the commands to the inverter. All of these need to be completed in a timely manner, before the motor's feedback readings become obsolete. The shorter the loop time, the faster the motor's response to changes, thus, less ripple and less energy being dissipated by the motor.

Advanced algorithms, such as Field Oriented Control (FOC) typically require fast computational and parallel processing performance which are difficult to meet using traditional DSPs or MCUs. FPGAs can provide a number of advantages over traditional processing devices, including higher performance, lower cost through greater on-chip integration of system components, robustness of solution, DSP capabilities and solution customization (Yvonne 2011).The increase in industrial energy efficiency during the past few years is largely due to a change in motor control technology. Using a power converter-based variable speed motor drive makes it possible to save up to 88% more energy than the previous generation of motor control applications (ABB review 2015).

1.1.2 The Variable Speed Drives in Induction Machine

VSDs accurately control the speed of standard AC induction or asynchronous motors. Induction motors are now the preferred choice for industrial motors due to their rugged construction, absence of brushes and ability to run at variable speeds

(Ravi et. Al, 2013). With VSDs, speed control with full torque is achieved from 0 rpm through the maximum rated speed and, if required, above the rated speed at reduced torque. VSDs manipulate the frequency of their output by rectifying an incoming AC current into DC, and then using voltage Pulse-Width Modulation (PWM) to recreate an AC current and voltage output waveform as shown by block diagram in Figure 2 (Shimpi 2011). However, this frequency conversion process causes 2% - 3% loss as heat in the VSD. The process also yields overvoltage spikes and harmonic current distortions (Ravi et. al 2013). The rotating field created by the induction motor stator windings is directly linked with the voltage frequency applied to the windings. VSDs can produce variable frequency and variable voltage waveforms. If these waveforms are applied to the stator windings there will be a shift of torque-speed curve, maintaining a constant pull-out torque, and the same slope of the linear operation region of the curve. In this way, the motor speed will be proportional to the applied frequency generated by the VSD (Ravichandrudu 2011).

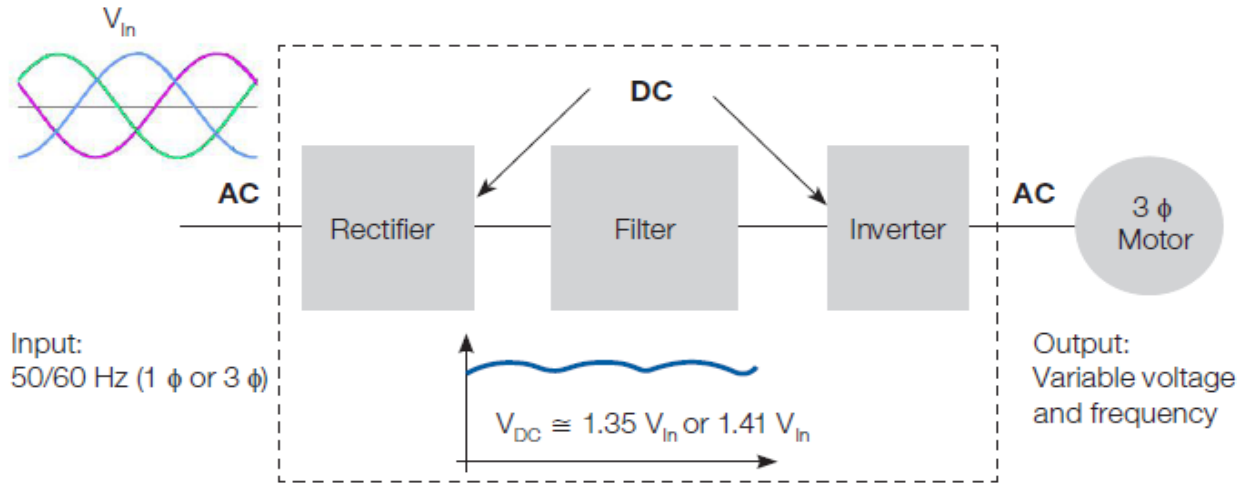

Figure 2. Operational Diagram of the VSD

1.1.3 Control Schemes Used in the Construction of VSDs

Digital PWM control and digital current control for AC drives was made possible by the advent of high performance and low-cost DSPs. The advantages are simple circuitry, software control and flexibility in adaptation to various applications. Most computation resources of the DSP must be devoted to generating the PWM signals and execution of current control algorithms. Employment of another DSP can resolve the problem but with enormous complication of the design process because of additional hardware and software (Tzou 1997).

Dynamic and ever progressing change in Very Large Scale Integration (VLSI) technology has radically affected the design process. The life cycle of modern electronic products may be even shorter than the design cycle. Therefore, the need for rapid prototyping poses a design challenge. In recent years, the development of ASIC technology has made it possible to integrate complex analogue and digital circuits by utilizing the libraries of basic circuit cell.

The ASIC approach provides a rapid, low-cost manufacturing solution for Integrated Circuits (ICs) with special applications. For sophisticated technology linked to a medium size marketing requirement, it is an optimal solution. Since the 1980s, ASIC technology has given rise to several new specialized technologies, including mask-programmable gate array, Cell-Based IC (CBIC), Programmable Array Logic (PAL), and Field-

Programmable Logic Array (FPLA) conversion.

With the advancement of the various technical aspects of ASIC, three major categories have emerged: CBIC, Gate Array (GA), and Programmable Logic Device (PLD). The CBIC has the longest lead time with highest number of gates, while the PLD allows the user to define the gate connections but with the lowest number of gates. The FPGA is a PLD developed by Xilinx, Altera and several other companies. The FPGA comprises thousands of logic gates, some of which are grouped together as a Configurable Logic Block (CLB) to simplify higher level circuit design. The advent of FPGA technology has enabled rapid prototyping of digital systems.
Pulse width modulated DC-AC converters may serve a wide range of applications in AC motor drives and ac power conditioning systems. The PWM strategy plays an important role in the minimization of harmonics and switching losses in these converters, especially in three-phase applications. In the past two decades, various PWM strategies, control schemes, and realization techniques have been developed. These PWM strategies were realized either by analogue circuit or microprocessor-based software control techniques. However, with the advance of high-frequency switching power devices, complex modulation schemes can no longer be realized even employing the most advanced digital signal processors, because of the high speed switching requirement. In recent years, motor control and powerICs employing ASIC/FPGA technology are receiving increased attention.
Utilizing FPGA to implement PWM methods has many advantages which are: fast prototyping, simple hardware and software configuration, switching frequency, and relieving the microprocessor from computational load. DSP/FPGA based control structure for air conditioning drives.

System on Programmable Chip (SoPC) is now in use for embedded system development. This promising new alternative technology enables designers to utilize a large FPGA that contains both memory and logic elements along with an Intellectual Property (IP) processor core. The advantages of SoPC design include reconfiguration, flexibility and short development cycle (Hall 2006).

1.1.4 Overview of a General FPGA Device.

The conceptual structure of an FPGA device is shown in Figure 3 (Chu 2012). A logic cell can be configured (i.e., programmed) to perform a simple function, and a programmable switch can be customized to provide interconnections among the logic cells. A custom design can be implemented by specifying the function of each logic cell and selectively setting the connection of each programmable switch. Once the design and synthesis are completed, a simple adaptor cable is used to download the desired logic cell and switch configuration of the FPGA device to obtain the custom circuit.

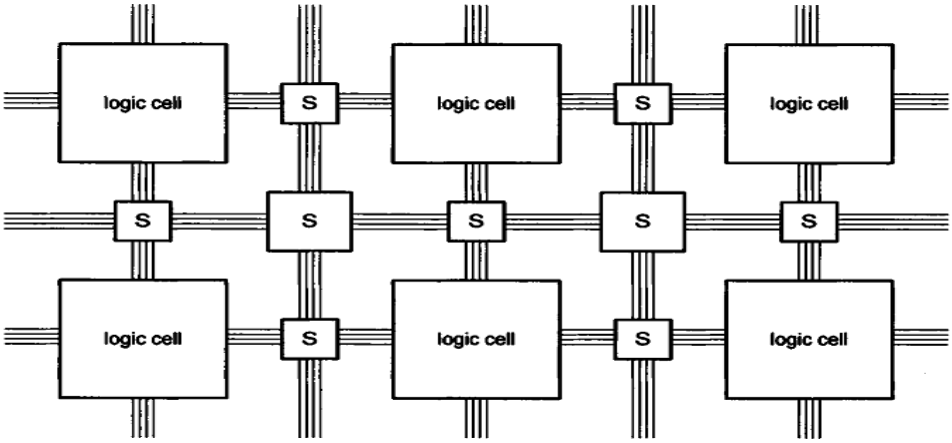

Figure 3. Structure of Altera Cyclone II FPGA Device

2. MATERIALS AND METHODS

2.1 Hardware Design and Implementation

This stage involved design and implementation of the control circuit and power circuit. The design on the control circuit involved describing the hardware on the FPGA chip, laying out the inverter switching devices, the gate driver circuits ,the digital input interface layout, the analogue input interface layout, LCD interface and keyboard circuitry layout. The design on the power stage included designing and building the AC to DC converter, the smothering stage and wiring the three phase voltage source inverter. The blocks inside the FPGA chip is shown in Figure 4.

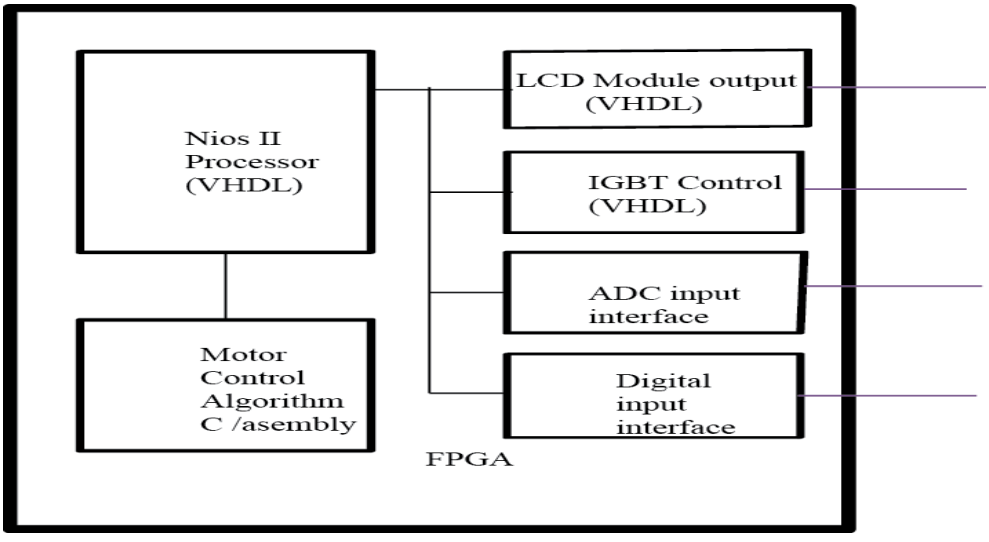

Figure 4. Proposed Blocks inside the FPGA Chip

2.2 Hardware Description on the FPGA

Defining the Nios II system, describing the IGBT module, the Analogue-to-Digital Converter (ADC) input interface and the digital input interface for the EP4CE22F17C6 FPGA chip on the DE0 Nano board was done using Quartus II

Subscription Edition (SE) version 13.0. A new project was created and set as the top level entity using the new project wizard. This top level entity defines interconnections between processor and modules. Connections to the FPGA physical I/O pins were linked to the top level entity. Nodes were also declared by right-clicking the target node and entering a name in the properties of development window. This eliminated many crossing nodes which would make the project difficult to debug.

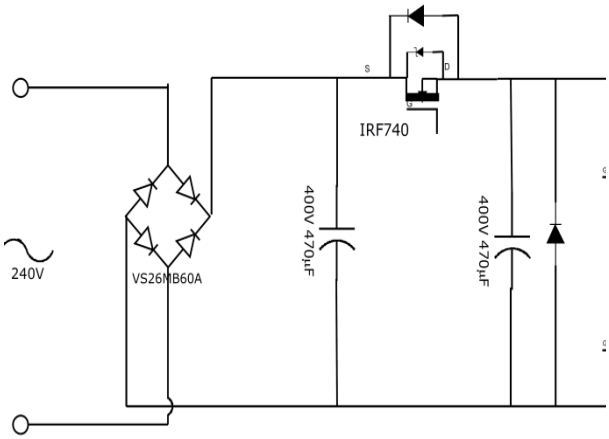

Figure 5. Power Circuit Schematic

The VS26MB60A 25A single phase rectifier was used for the convertor stage. On this stage 220V AC is converted to 315 V DC. The switching devices that were used were the IRF740 MOSFET. Two 400V 470 µF capacitors are used at the smoothing stage. A buck converter is used to vary the voltage across the three phase inverter to maintain a constant voltage to frequency ratio across at the inverter output. A one horse power (745.7W) three phase induction is connected at the output of the motor.

2.3 Analogue Input Interface Design

A potential divider was used to keep the input from the PLC within operating ranges. A blocking diode was used to filter out the negative half (-10 to 0V) output from the PLC. The analogue input interface requires to be calibrated which is the case with existing VSDs.

2.4 Power Circuit Design

The power circuit design consisted of four stages: the converter, smoothening stage, the buck converter and the three phase voltage source inverter. The schematic of the power circuit is shown in Figure 5.

2.5 Digital Frequency Variation

The digital input PIO was read for every program cycle. Figure 6 illustrates the digital frequency variation algorithm.

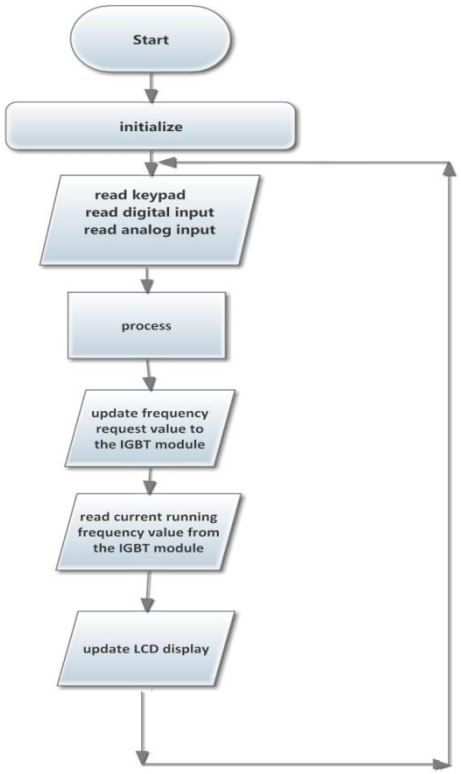

Figure 6. Flow Chart of the Nios II Program Flow

2.6 PLC Programming

A new ladder logic programme was created using RS Logix 500 pro to manipulate the digital and analogue outputs of the PLC from

internal memory scaled parameters. Instruction was used to scale input frequency values of 0- 50 Hz to an integral analogue output value of 0- 32767. RSLogix 500 window is shown is Figure 7.

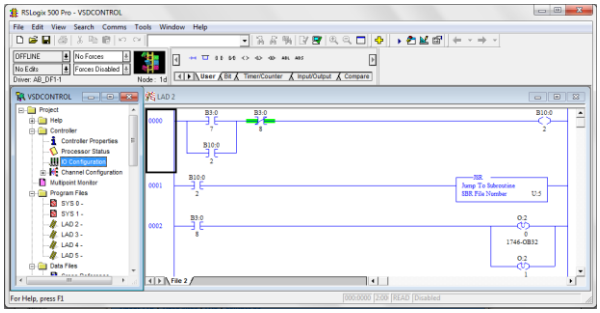

Figure 7. Programming the PLC using RSLogix 500

2.7 Human Machine Interface Configuration

Visual Studio 2013 is used to fabricate the Human Machine Interface (HMI) application as shown in Figure 8. The visual basic Advanced HMI project is customized to create a simple motor control window. An OPC communication driver is configured for the window. This driver is linked to the RSLinx OPC server UNTITLED topic. Buttons and switches are used to toggle internal memory files of the PLC. Analogue meters are used to represent both the digital and analogue speed request to the VSD.

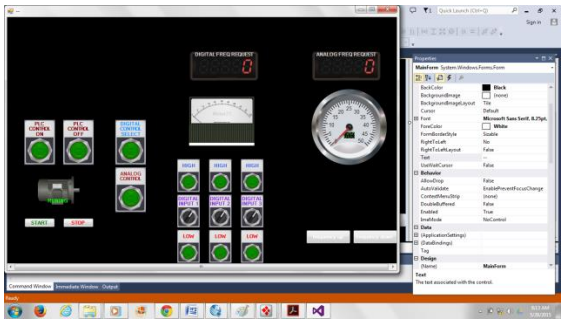

Figure 8. Developing the HMI application using Visual Studio 2013

3. RESULTS

The designed VSD was performance tested. The results of simulations and practical tests are shown in this section.

3.1 Insulated-Gate Bipolar Transistor Module Simulation

The Insulated-Gate Bipolar Transistor (IGBT)module has been simulated using Model Sim Altera Editing. A test bench was written in VHDL and the result of the simulation is shown in Figure 9. The bottom three waveforms from the clock signal are shown in Figure 10. The gating signal to switching devices in the same leg can be identified since one waveform is the other one inverted (A and Not A for example).

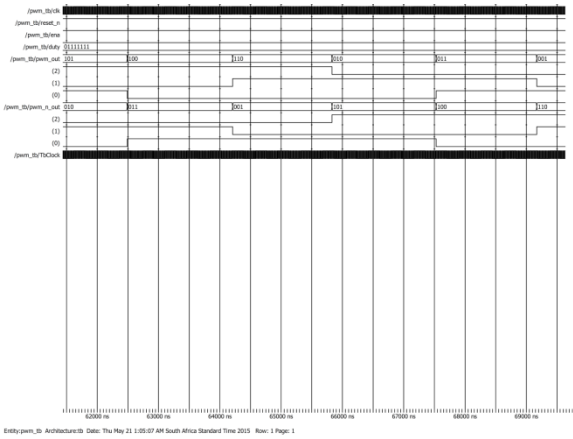

Figure 9. Altera Stater Edition Showing the IGBT Module Simulation

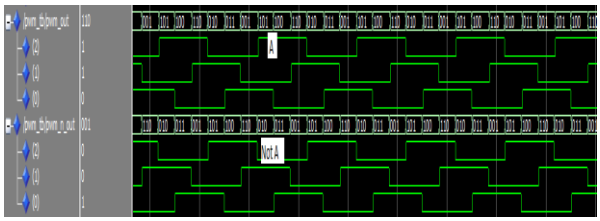

Figure 10. Output of Simulating Three Phase PWM Signal

3.2 Gate drive signal testing

An oscilloscope was used to test the gating signals. Figure 11 shows gating signals (channel 0 yellow and channel 1 blue) for two switching devices in the same leg.

When one switching device is on, the other one should be off to avoid shorting of the DC bus which will destroy the switching devices. Also a dead time is allowed to cater for the fall time and the rise time for the switching MOSFETS(Power MOSFET 2011). This dead time is illustrated in Figure 12.

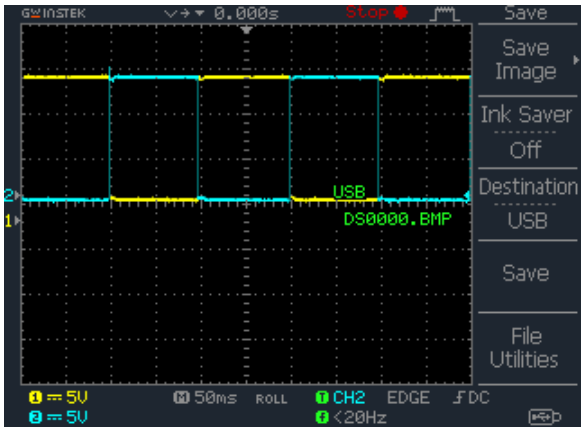

Figure 11. Oscilloscope Trace for Gating Signals to Switching Devices of the Same Leg

The gating signals for two switching devices in different legs are shown in Figure 13 and Figure 14. The signals are 120 degrees out of phase as required.

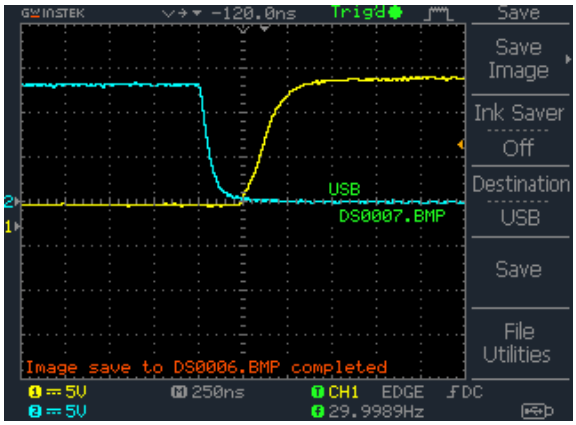

Figure 12. Signal Showing Dead Time

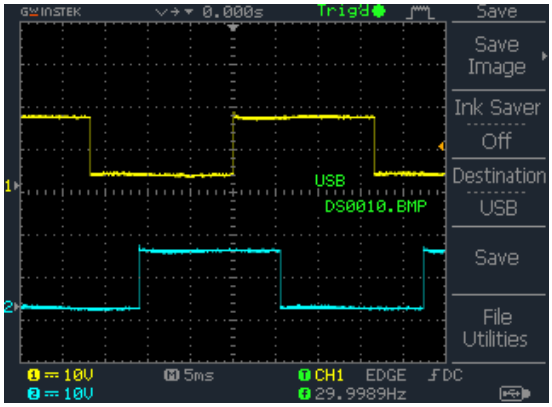

Figure 13. Gating Signals for Two Switching Devices on Different Legs

3.4 Output Voltage

The setup shown in Figure 14 was laid out to observe the variation of output voltage to the motor with frequency. Two voltmeters were used to measure the output phase to phase voltage between two phases. The results are depicted on Table 1.

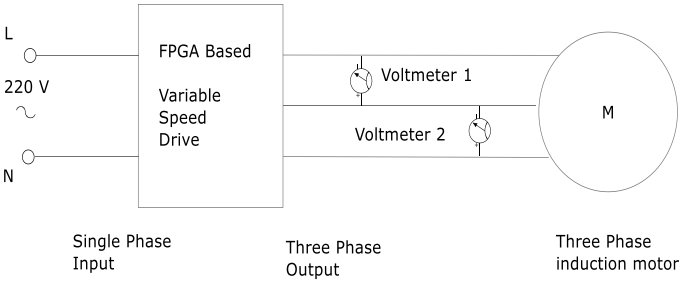

Figure 14. Experiment to Determine variation of Voltage with Frequency

Table 1. Variation of Voltage with Frequency

Frequency [Hz]	Voltmeter 1st reading [V]	Voltmeter 2nd reading [V]	Average Phase Voltage [V]	Voltage- to-Frequency Ratio
44	180	170	175	3.98
40	152	144	148	3.7
50	199	177	188	3.76
32	133	119	116	3.63

4. CONCLUSIONS

The design and implementation of the FPGA based variable speed drive has been presented. The results obtained from simulations and practical tests have shown the feasibility of designing variable speed drives using FPGAs. For the system to be applied on an industrial scale the inverter stage must be replaced by IGBT modules. PWM modulation must be replaced by Space Vector Pulse Width Modulation. Tools like Drive on Chip and motor control IP Suite can also be used (Altera cooporation, 2015). Gate driver circuits can also be eliminated through the use of modules with inbuilt gate driver circuits.

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